LDPC Compiler For NAND Flash and SSD Controllers

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Proton Read Channel

- LDPC-Based Read Channel provides significant improvement in NAND Flash longevity.
LDPC Compiler

- LDPC Compiler supporting a wide range of data-rates
  - 50MB/s to 3.5GB/s for a single LDPC instance (in 40nm process)

- List of parameters selected prior to instantiation:
  - Codeword size (Macro-level: 1KB vs. 0.5KB vs. 2KB, etc.)
  - Several parameters for degree of parallelism and memory access options

- After compilation, each instance is supporting:
  - Simultaneous support for different amounts of parity/code rate
  - Simultaneous support for several LDPC codes
  - On-the-fly switching from one LDPC code to another
  - Each matrix can be an arbitrary LDPC matrix subject to certain constraints
LDPC Decoder Core Examples

- Codeword size is 1KB
- Total power is measured for TT, 0.9V, 25C
- TSMC 40G process

<table>
<thead>
<tr>
<th>Decoder Throughput</th>
<th>Clock Frequency</th>
<th>LDPC Compiler Options</th>
<th>Gate Count (KG)</th>
<th>Memory Size</th>
<th>Total Power (Gates+Memory+leakage)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Beginning-of-Life</td>
</tr>
<tr>
<td>800 MB/s</td>
<td>450 MHZ</td>
<td>Option set 4 CW=1KB</td>
<td>158.6</td>
<td>17.9KB</td>
<td>46mW</td>
</tr>
<tr>
<td>111 MB/s</td>
<td>250 MHZ</td>
<td>Option set 2 CW=1KB</td>
<td>36.6</td>
<td>17.9KB</td>
<td>5mW</td>
</tr>
</tbody>
</table>
More LDPC Examples

- LDPC Decoder cores (compiler output) examples for ASIC implementation under various conditions.

<table>
<thead>
<tr>
<th>LDPC Compiler Options</th>
<th>Technology Library</th>
<th>Frequency (MHz)</th>
<th>Throughput (MByte/s)</th>
<th>Gate Count (KG)</th>
<th>Memory (KByte)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TSMC 40nm G HVT ONLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Option set 1, CW=1KB</td>
<td>9T</td>
<td>250</td>
<td>111</td>
<td>36.6*</td>
<td>17.9</td>
</tr>
<tr>
<td>Option set 2, CW=1KB</td>
<td>9T</td>
<td>400</td>
<td>222</td>
<td>46.2*</td>
<td>17.9</td>
</tr>
<tr>
<td>Option set 3, CW=1KB</td>
<td>9T</td>
<td>600</td>
<td>534</td>
<td>70.4*</td>
<td>20.5</td>
</tr>
<tr>
<td>Option set 4, CW=1KB</td>
<td>9T</td>
<td>500</td>
<td>895</td>
<td>158.6*</td>
<td>17.9</td>
</tr>
<tr>
<td>Option set 5, CW=1KB</td>
<td>9T</td>
<td>500</td>
<td>1780</td>
<td>301.4*</td>
<td>20.5</td>
</tr>
<tr>
<td>Option set 5, CW=1KB</td>
<td>12T</td>
<td>1000</td>
<td>3560</td>
<td>391.8*</td>
<td>20.5</td>
</tr>
</tbody>
</table>

* Gate count is measured based on two input NAND gate
ASIC, eASIC and FPGA implementation and integration are supported

ASIC implementation
- Cadence Design Flow
- TSMC libraries
- Trial place and route at IP/Block level

eASIC implementation
- LDPC Compiler is run with a custom option set for eASIC
- Full integration with eASIC design flow, design implemented with clock frequency up to 500MHz.

FPGA implementation
- LDPC Compiler is run with a custom option set for FPGA
Sufficient Iterations for End-of-Life

- LDPC Decoder computational load and power consumption increase towards the End-of-Life of SSD:
  - Average iterations=3.5
  - Power=172mW/GB/s*
  - Average iterations=1
  - Power=57mW/GB/s*
  - *TSMC 40G

- LDPC Compiler guarantees sufficient iterations for End-of-Life
  - Guaranteed sustained 3.5 LDPC iterations for quoted data-rates
  - Maximum iteration limit is programmable and is typically much higher (e.g. 8-128)
LDPC For Conventional Read

- Full-power LDPC decoder is used for conventional read ("hard-decision decoding")
- This reduces the occurrence rate of soft-information read
- Example of LDPC Correction Capability:

<table>
<thead>
<tr>
<th>Method</th>
<th>User Bytes</th>
<th>Parity Bytes</th>
<th>Average bit errors corrected</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCH,  T=70</td>
<td>1KB</td>
<td>123</td>
<td>70</td>
</tr>
<tr>
<td>LDPC</td>
<td>1KB</td>
<td>123</td>
<td>73</td>
</tr>
<tr>
<td>Hard-Input Decoding</td>
<td>1KB</td>
<td>123</td>
<td>&gt;186 (=ER @ optimal Vth)</td>
</tr>
<tr>
<td>LDPC</td>
<td>1KB</td>
<td>123</td>
<td>&gt;490 (=ER @ nominal Vth)</td>
</tr>
</tbody>
</table>
From LDPC to Flash Read Channel

- Significant testing and system optimization required for full Flash Read Channel Solution – LDPC is only a component

- Read Channel testing on various Flash Geometries: 2X/2Ynm, 1Xnm
  - “Special Commands” from different Flash manufacturers

- Testing on full manufacturing yield distribution
  - Flash samples from production line
  - “Bad Samples” from production line